A Current-mode DC-DC Converter using a Quadratic Slope Compensation Scheme

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Abstract— A quadratic slope compensation scheme for a current-mode DC-DC converter to obtain stable frequency characteristics without depending on the input and output voltages is proposed. A 5 MHz and 500 mA buck DC-DC converter with input voltages ranging from 3.3 V to 2.5 V and with output voltages ranging from 2.5 V to 0.5 V was fabricated by using a 0.35 μm CMOS process to verify the effectiveness of the scheme. Little variation of frequency characteristics at frequencies above 200 KHz for the various input and output voltages was observed.

I. Introduction

DC-DC converters have become more important with the evolution of mobile equipment. In such applications, a short cycle time of power on and off of the circuits on boards is required. The use of a current-mode DC-DC converter is appropriate because it has a larger frequency bandwidth than the voltage-mode DC-DC converter, and, therefore, the transient response for the load voltage and current changes is fast. However, a compensation slope is needed in the current feedback loop of the current-mode DC-DC converter, a block diagram of which is shown in Fig. 1 [1]. There, a linear compensation slope is commonly used, but the frequency bandwidth changes when the input and output voltages change and overcompensation to guarantee the stability for all the conditions becomes necessary [2]. In this paper, a quadratic slope is proposed as the best suited compensation slope to a current feedback loop of a current-mode DC-DC converter. The independence of the frequency bandwidth of the input and output voltage changes was verified with adoption of the quadratic slope.

II. The best fit compensation slope for a current-mode DC-DC converter

Fig. 2 shows two signals that control the duty ratio D in a current-mode DC-DC converter. D decides the on time of the output transistor M_p in Fig. 1. V_i represents the current in the inductor L in Fig. 1, although it is converted to voltage, while V_c represents the difference voltage between the output voltage V_{out} and the reference voltage V_{ref}. When the output current I_{out} suddenly changes, V_i changes by ΔV_1. At the end of the one clock period T_s of the DC-DC converter, the voltage difference between the old V_i and new V_i, which is shown in the dotted line in Fig. 2, becomes ΔV_2. Fig. 2(a) shows the condition where the duty ratio D is greater than 50 %. In this case, ΔV_2 becomes larger than ΔV_1, and the DC-DC converter loses the control of the output voltage.

In order to avoid the loss of control of the output voltage, the linear compensation slope $-m_c$ which changes V_c as time increases, as shown in Fig. 2(b), is commonly adopted. Then,

$$\frac{\Delta V_2}{\Delta V_1} = -\frac{m_2 - m_c}{m_1 + m_c}, \tag{1}$$

is derived. If $m_c > (m_2 - m_1)/2$, then equation (1) has the value of less than one. This means that ΔV_2 becomes smaller than ΔV_1 at the end of a clock period and the system is stable. By further modifying the condition with the relationship of $m_1 D = m_2 (1 - D)$ and $m_1 = K_{cfb} \frac{V_{in} - Vout}{L}$, we obtain

$$m_c > \frac{(2D - 1) V_{in}}{2L} K_{cfb}, \tag{2}$$

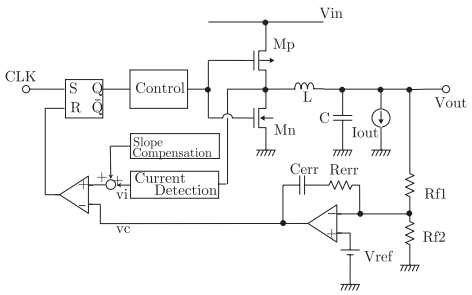

Fig. 1. The block diagram of the current-mode DC-DC buck converter.

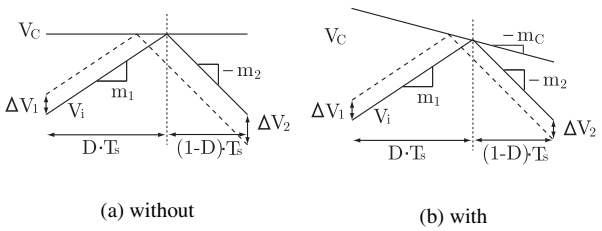

Fig. 2. Two duty control signals V_i and V_c without and with a compensation slope when the ΔV_1 change in V_i occurs.

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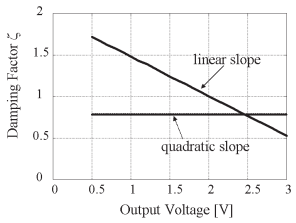
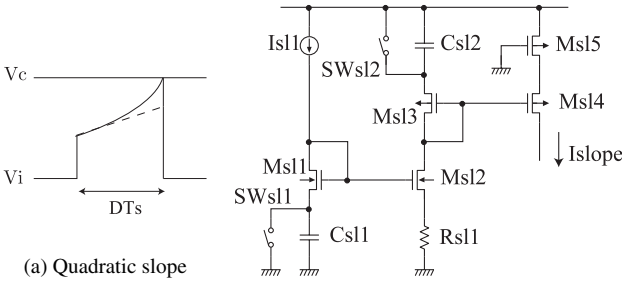


Fig. 3. Comparison of the linear slope and the quadratic slope.



(a) Quadratic slope

(b) The circuit

Fig. 4. The circuit to generate the quadratic slope.

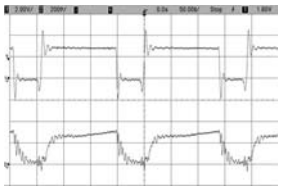


Fig. 5. Waveforms of the IC output and the quadratic slope V_i.

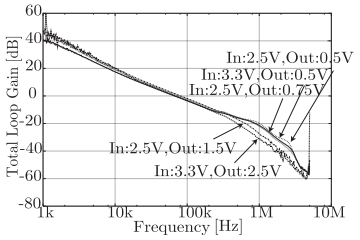


Fig. 6. Loop frequency characteristics of the DC-DC converter.

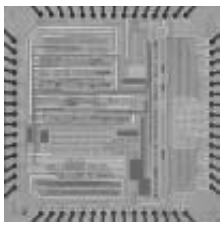


Fig. 7. The micrograph of the test chip

TABLE I
PERFORMANCE OF A TEST CHIP

Input Voltage	3.3V $\sim$ 2.5V
Output Voltage	2.5V $\sim$ 0.5V
Max. Load Current	500 mA
Load Current Change (200 mA $\sim$ 20mA)	50 μs within 50 mV
Output Ripple	-48 dBm (2nd Harmonic)
Efficiency (In:3.3 V, Out:2.5V)	85 % (Iout = 100 mA)
Process	0.35 μm CMOS
Max. Voltage Tolerance	3.3V

where K_{cfb} is the transformation factor of the inductor current into V_i. Equation (2) indicates that the compensation slope m_c is in proportion to the duty ratio D. This means that V_c needs to change in the quadratic manner as D increases.

The difference in the frequency characteristics of the current feedback loop between the linear slope and the quadratic slope appears as the difference of the output voltage dependence of the loop damping factor ζ as shown in Fig. 3. The quadratic slope realizes the constant ζ value which is close to 1/2 and, therefore, the stable frequency characteristics.

III. The quadratic slope generation circuit

In actual, V_i instead of V_c changes in the quadratic manner, as shown in Fig. 4(a). The current which is proportional to the time in the quadratic manner is produced by time integrating the constant current twice by capacitors C_{sl1} and C_{sl2}, as shown in Fig. 4(b). C_{sl1} integrates the constant current I_{sl1} and the resultant voltage is then converted into current by R_{sl1} and is applied to C_{sl2}. C_{sl2} again integrates the current. The voltage across C_{sl2} is then converted to current by the equivalent source resistor M_{sl5} at the source terminal of a transistor M_{sl4}, and a quadratic current I_{slope} in Fig. 4(b) is obtained. V_i is produced by using this I_{slope}.

IV. Experimental results

A test chip adopting the quadratic slope compensation scheme was designed, fabricated and evaluated by using a 0.35 μm CMOS process. The clock is 5MHz. Fig. 5 shows waveforms at the out terminal of the IC where the inductor L connects, and the V_i in Fig. 4(a) when V_{in}, V_{out} and I_{out} are 3.3V, 2.5V and 250mA, respectively. The slope in V_i should be quadratic. Fig. 6 is the open-loop frequency characteristics with various input and output voltages from 3.3V to 2.5V for the input and from 2.5V to 0.5V for the output. The duty ratio D becomes more than 50 % for the condition when $V_{in} = 3.3$V and $V_{out} = 2.5$V, and $V_{in} = 2.5$V and $V_{out} = 1.5$V. The constant frequency characteristics have been realized. Fig. 7 is the micrograph, and Table 1 summarizes the overall performance of the test chip.

V. Conclusion

The quadratic slope compensation scheme has been adopted to a MOS current-mode buck DC-DC converter, and the constant loop frequency characteristics were obtained.

Acknowledgements

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References

[1] R.D.Ridley, "A new, continuous-time model for current-mode control," IEEE Trans. Power Electron., vol.6, no.2, pp.270-280, April 1991.

[2] H.Sakurai and Y.Sugimoto, "The Analysis and the Design of a Current-mode PWM Buck Converter by adopting the output-voltage independent Second-order Slope Compensation scheme," IEICE Trans. Fundamentals, vol.E88-A, no.2, pp.490-497, February 2005.